Today, every manufacturer includes more features to their products while maintaining low price to increase their strength in the market. Both low power consumption and cost reduction is a significant challenge for System on Chip (SoC) Designers.

In an effort to design complex SoC circuits with ever ultra low power consumption, RF Silicon has designed its own building blocks, including ultra low power STSCL Standard Cell Library and Memories.

**Standard Cell Library**

RF silicon has designed large number of libraries, specifically to achieve their low power objective. STSCL Standard Cell library is one with ultra low power optimization.

**Features**

- Fully customizable standard cell library
- New Layout Architectures
- Controlled output voltage swing
- Single metal layer design for high routing utilization
- Low supply voltage, because all the transistors operate in sub threshold.
- Ultra Low Power and Balanced architectures
- Exceeds foundry DFM (Design For Manufacturability) requirements resulting in highest yields
- Multiple drive strengths
- Operation over a wide range of frequencies
- Less sensitive to the process and temperature variations. Due to their differential topology, supply voltage variation has minor effect
- Uniform and common power management scheme
Ultra Low Power

STSCCL Standard Cell Library

Sub Threshold Source Coupled Circuit

- Very low power consumption
- Applicable in a very wide frequency range
- Use a novel load device concept to implement controllable and ultra high value resistances.
- Using the high value resistance to implement very low power digital and analog circuits.
- Controlled swing voltage defines the speed of operation
- Circuits are re-usable for different system applications.

Controlled High Value Resistance

Controlled High Value Resistance

I-V Characteristics of Controlled High Value Resistance

STSCCL Inverter Schematics

Out Put Voltage Swing

List of Deliverables

- Transistor Net List (CDL)
- Layout (GDS)
- Abstract File (LEF)
- Synthesis Models (.lib)
- Simulation Models VHDL/Verilog)
- Validation Report
- Quality and Assurance (QA) Report
- Cap Data Base
- Data Sheet